**Bulk Driven Non-Tailed Operational Transconductance Amplifier for Ultra-Low Power Applications**

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**Introduction**

In recent years, the interest in ultra-low power analog circuits has been increased widely. Increased demand for power-efficient low power solutions used in medical or wearable devices for biomedical applications. Low power will decrease the power dissipation in both analog and digital devices.

One of the most widely used analog building blocks in CMOS circuits is the operational transconductance amplifier (OTA). Several Ultra Low Voltage OTAs have been proposed in the different literature in recent years for biomedical applications. These circuits can operate even from the deep sub 0.5 voltage supply.[1]

These OTAs are most of the time based on subthreshold bulk-driven transistors. even the bulk-driven transistors show several issues such as lower transconductance, larger input noise, and offset, still, this technique seems to be very efficient when the supply voltage is very low and input mode common-mode range is required at the same time.

Here the bulk of the gate-driven MOS amplifier is used as a control terminal to lower threshold voltage and provide common-mode control and increases the ICMR. A combination of the bulk-driven nontailed differential stage with multipath zero cancellation compensation technique has been provided to obtained rail to rail ICMR. This OTA is compact, easy to design, and offers better power efficiency and a common-mode rejection ratio.[2]

**Circuit Diagram:**

The circuit proposed is shown in Fig. 1, which is a two-stage OTA with an additional feedforward path to recompense for the right-half-plane (RHP) zero introduced by the Miller compensation capacitance Cc. The input stage(M1-M4) is based on non-tailed bulk-driven differential pair with cross-coupled MOS for gain enhancement. The circuit can operate with a very low supply voltage of 0.5V resulting in high CMRR, power supply rejection ratio (PSRR), ICMR with low power dissipation. The circuit is simulated with LTspice.

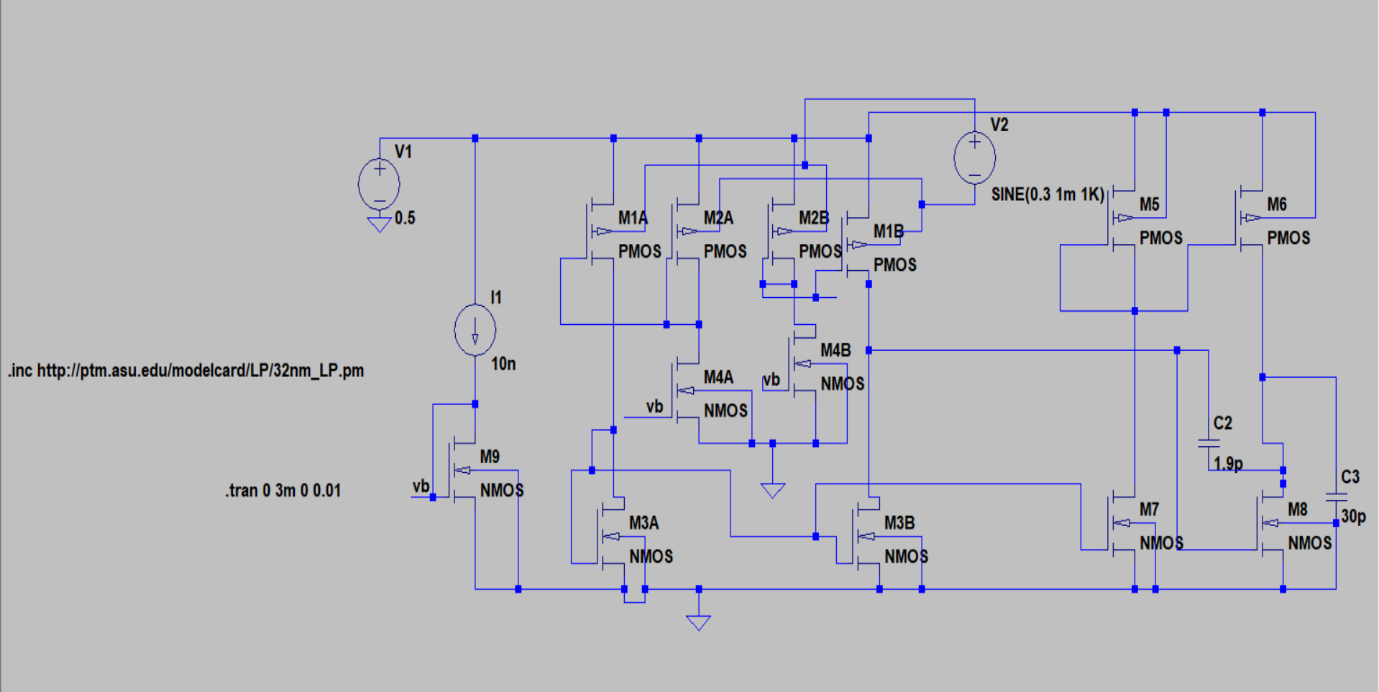


Fig 1: Circuit Diagram of Bulk driven OTA

**Transistor Aspect Ratio:**

An aspect ratio of all the transistors is given below in the table.

Table I: Aspect Ratio

|  |  |  |  |
| --- | --- | --- | --- |
| **Device** | **W/L(µm/µm)** | **Device** | **W/L(µm/µm)** |
| M1A, B, M2A, B | 15/1 | M6 | 1400/0.4 |
| M4A, B | 15/0.5 | M7 | 41.2/1 |
| M3A, B | 400/0.5 | M8 | 200/1 |
| M5 | 300/0.4 | M9 | 15/0.5 |

**Small-Signal Performance**: The open-loop dc voltage gain of the OTA is not significantly affected by the feed-forward path and can be expressed as [3]

Avo = 2gmb1 \* gm8 / (gds6 + gds8 )\* (gds1 + gds3 ) **………(1)**

while the GBW product is represented by equation (2),

GBW = 2*g*mb1 / Cc **…………(2)**

**Tools Used**

**Synopsis Custom Compiler:**

The Synopsys Custom Compiler™ design environment is a modern solution for full-custom analog, custom digital, and mixed-signal IC design. As the heart of the Synopsys Custom Design Platform, Custom Compiler provides design entry, simulation management and analysis, and custom layout editing features. This tool was used to design the circuit on a transistor level.

**Synopsys Primewave:**

PrimeWave™ Design Environment is a comprehensive and flexible environment for simulation setup and analysis of analog, RF, mixed-signal design, custom-digital, and memory designs within the Synopsys Custom Design Platform. This tool helped in various types of simulations of the above-designed circuit.

**Synopsys 28nm PDK:**

The Synopsys 28nm Process Design Kit(PDK) was used in the creation and simulation of the above-designed circuit.

**Pre-Layout Schematics:**

## **Bulk has driven OTA schematic**: Fig 2 shows the transistor level schematic, which is made in Synopsys IC compiler using a 28nm technology file.

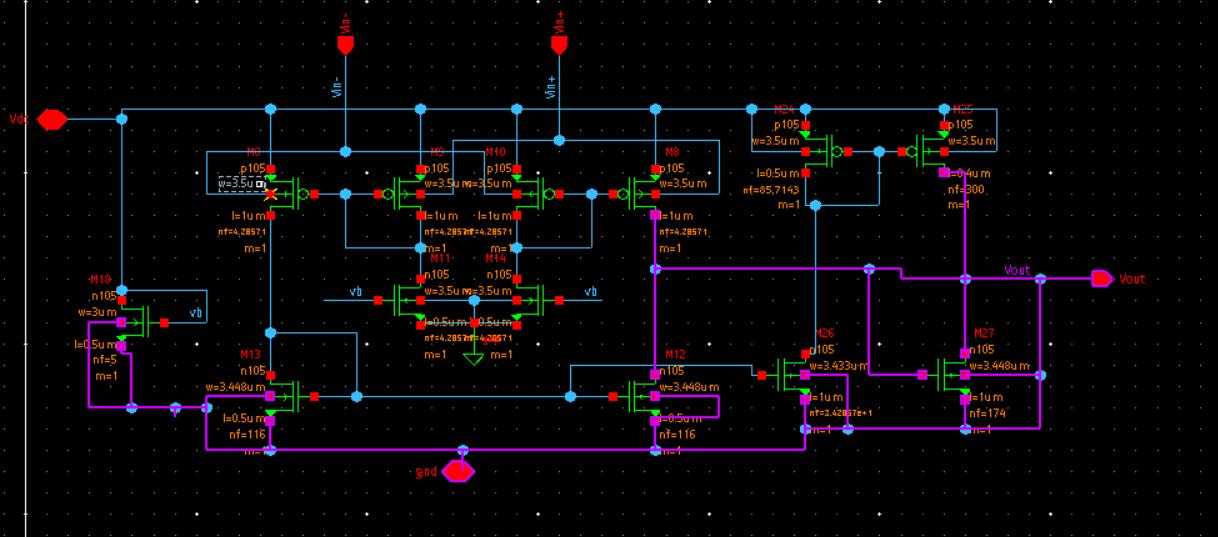


Fig 2: Schematic of OTA

**Symbol:** Fig 3 represents the symbol of the OTA with input-output ports and supply rails.

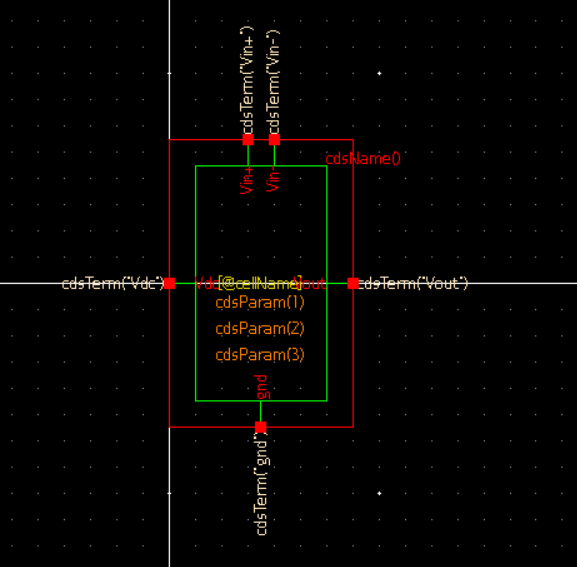


Fig 3: Symbol of OTA

# Gain analysis: As shown in Fig 4, gain analysis is Performed through AC analysis by giving the Sinewave at the input and measuring the gain of the amplifier is 37.6 dB.

# Fig 4: Gain of OTA

# Power dissipation: Power dissipation is calculated through DC operating points by performing DC analysis as shown in Fig 5. The average power dissipation was measured as 5.70nW with Vdd=0.5V and a Bias current of 10nA.

# Fig 5: Power dissipation

# Slew Rate: Slew rate calculation is done in the Synopsys prime wave using Transient analysis as shown in Fig 6.

# Fig 6: Slew Rate

# Netlist of the circuit

# Observation

# A solution of ultra-low-voltage OTA is proposed with a 28nm technology node, which contains a bulk-driven differential stage and gives good power efficiency. Through the AC analysis gain of the circuit is measured and power dissipation is also calculated which gives the 37.5 dB of gain with 65.744nW power dissipation.

# Author

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# Acknowledgments

# • Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd. • Cloud-Based Analog IC Design Hackathon • [Synopsys India](https://www.synopsys.com/) • VLSI System Design (VSD) Corp. Pvt. Ltd India • Chinmay panda, IIT Hyderabad

# References

[1]Abdelfattah O, Roberts GW, Shih I, Shih YC. An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range.  IEEE Transactions on Circuits and Systems I: Regular Papers. 2015 Sep  25;62(10):2380-90.

[2] Kulej T, Khateb F, Arbet D, Stopjakova V. A 0.3-V high linear rail-to rail bulk-driven OTA in 0.13 μm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs. 2022 Jan 18.

[3] Kulej T, Khateb F. A compact 0.3-V class AB bulk-driven OTA. IEEE  Transactions on Very Large Scale Integration (VLSI) Systems. 2019 Sep  13;28(1):224-32.